

FILE 'USPAT' ENTERED AT 13:00:30 ON 19 JUL 1999

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* * * * *
*       U. S.   P A T E N T   T E X T   F I L E       *
*
*   THE WEEKLY PATENT TEXT AND IMAGE DATA IS CURRENT   *
*   THROUGH July 13,1999                                *
*
*
* * * * *
```

=> s (wire# or conductor# or line#) (p) bundl### (p) process###

```
      363565 WIRE#
      195413 CONDUCTOR#
      1500513 LINE#
      49517 BUNDL###
      1291644 PROCESS###
L1      2163 (WIRE# OR CONDUCTOR# OR LINE#) (P) BUNDL### (P) PROCESS###
```

=> s l1 (p) cell#

```
      277475 CELL#
L2      49 L1 (P) CELL#
```

s (wire# or conductor# or line#) (3a) bundl###

363565 WIRE#
195413 CONDUCTOR#
1500513 LINE#

49517 BUNDL###
L7 6112 (WIRE# OR CONDUCTOR# OR LINE#) (3A) BUNDL###

=> s 17 (p) process###

1291644 PROCESS###
L8 697 L7 (P) PROCESS###

=> s 18 (p) cell#

277475 CELL#
L9 11 L8 (P) CELL#

FILE 'USPAT' ENTERED AT 13:47:16 ON 19 JUL 1999

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* * * * *
*       U. S.   P A T E N T   T E X T   F I L E       *
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*   THE WEEKLY PATENT TEXT AND IMAGE DATA IS CURRENT   *
*   THROUGH July 13,1999                               *
*
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* * * * *
```

=> s (wire# or conductor# or line#) (p) (processor# or processing(w)unit#)
(p) cells

```
      363565 WIRE#
      195413 CONDUCTOR#
1500513 LINE#
      136604 PROCESSOR#
      513545 PROCESSING
      915650 UNIT#
      188722 CELLS
L1      1477 (WIRE# OR CONDUCTOR# OR LINE#) (P) (PROCESSOR# OR PROCESSIN
G(W      )UNIT#) (P) CELLS
```

d 1,4 cit ab

1. 5,418,952, May 23, 1995, Parallel processor cell computer system; Richard E. Morley, et al., 712/14; 364/229, 229.2, 230.1, 230.3, 231.9, 232.1, 280.7, 281.3, 281.4, DIG.1; 712/20 [IMAGE AVAILABLE]

US PAT NO: 5,418,952 [IMAGE AVAILABLE]

L6: 1 of 6

ABSTRACT:

A computer system especially for solution of real time inference problems is disclosed. The system includes a systolic cellular **processor** which provides predictable and responsive real time operation and fine grain **programmability**. The system comprises a plurality of separate **processor cells** each having its own local memory, the **cells** running simultaneously and operative to execute their respective **program** instructions. A global memory is coupled via a global **bus** to the **processor cells** and provides data to the **cells** and stores data from the **cells**. The **bus** provides effectively simultaneous access of all **cells** to the global memory. A further feature of the system is a novel parallel **programming** language using English syntax and which provides synchronous and predictable binding of code to each cell. A graphic work station is provided as a user interface to provide visual access to each cell or to cell groups for ease of control. The system can also function to emulate large scale integrated circuit **processors** by reason of the fine grain **programmed** operation of the system.

4. 4,852,048, Jul. 25, 1989, Single instruction multiple data (SIMD) cellular array processing apparatus employing a common bus where a first number of bits manifest a first bus portion and a second number of bits manifest a second bus portion; Steven G. Morton, 712/11; 364/228.6, 229, 229.4, 231.9, 232.8, 232.9, 238, 240, 240.1, 244, 244.6, 244.8, 244.9, 245, 245.3, 247, 247.8, 256.3, 265, 266.3, 267, 267.7, 268, 268.9, 280, 280.2, 280.3, DIG.1; 712/22 [IMAGE AVAILABLE]

US PAT NO: 4,852,048 [IMAGE AVAILABLE]

L6: 4 of 6

ABSTRACT:

In a cellular array including a matrixed array of processing elements, the processing elements are controlled by software to overcome manufacturing defects, to cooperate together to form words of varying size and to replace **cells** that become defective during the lifetime of the **processor**. These **cells** communicate with memory external to the chip via a time division multiplex **bus**. The **bus** is 32-bits wide and each cell is connected to both the upper half and the lower half of the **bus**. Configuration bits that are loaded into a cell cause communication over the top half or the bottom half of the **bus** according to the significance of the bits placed in the **cells**. Words between 16-bits and 246-bits in length may be formed in a case where 20 such **cells** are implemented on a single chip with four of the **cells** being deemed to be spare parts. For simplicity, typical word sizes would be 2n.times.16 bits although in principle any multiple of 16-bits may be obtained. Each cell contains a 16-bit multiport RAM providing general purpose registers for use by the **programmer** as well as systems registers. The systems registers accommodate the **processor** status word, a multiplier quotient register, a full-function arithmetic logic unit and path logic to connect the **cells** together and control the flow of information through the path logic according to the

3. 5,763,944, Jun. 9, 1998, Semiconductor device having a reduced wiring area in and out of data path zone; Hisao Harigai, 257/690, 688, 689, 691, 693, 700 [IMAGE AVAILABLE]

US PAT NO: 5,763,944 [IMAGE AVAILABLE]

L9: 3 of 11

ABSTRACT:

A semiconductor device formed on a semiconductor chip includes a signal processing unit composed of a plurality of signal processing cells arranged side by side in a horizontal direction, and a plurality of input/output cells each connected to a corresponding one of the signal processing cells in a one-to-one relation. The signal processing unit is located near to one corner of the semiconductor chip, and the input/output cells are uniformly distributed and located along two sides defining the above mentioned corner. Each of the signal processing cells is configured to make it possible that a wiring conductor connecting between the signal processing cell and a corresponding one of the input/output cells is taken out either in an upward vertical direction or in a downward vertical direction from the signal processing cell, in accordance with the side of the semiconductor chip along which the corresponding input/output cell is located.

instruction being executed.

d cit ab

1. 5,113,498, May 12, 1992, Input/output section for an intelligent cell which provides sensing, bidirectional communications and control; Shabtai Evan, et al., 710/8; 364/221, 221.1, 228, 228.1, 231.8, 232.2, 232.8, 237.8, 238.3, 240, 240.8, 240.9, 241.9, 242.94, 242.96, 244, 244.3, 244.6, 244.9, 247, 247.2, 247.5, 247.6, 247.7, 247.8, 254, 254.5, 259, 259.1, 259.3, 259.5, 260, 260.3, 260.4, 260.81, 262, 262.3, 262.4, 262.9, 270, 271, 271.4, 271.5, 281.3, 284, 284.3, 284.4, DIG.1 [IMAGE AVAILABLE]

US PAT NO: 5,113,498 [IMAGE AVAILABLE]

L16: 1 of 1

ABSTRACT:

A network for providing sensing, communications and control is described. A plurality of intelligent **cells** each of which comprises an integrated circuit having a **processor** and input/output section are coupled to the network. Each of the **programmable cells** receives when manufactured a unique identification number (48 bits) which remains permanently within the **cell**. The **cells** can be coupled to different media such as power **lines**, twisted, pair, radio frequency, infrared ultrasonic, optical coaxial, etc., to form a network. The preferred embodiment of the **cell** includes a multiprocessor and multiple I/O subsections where any of the **processors** can communicate with any of the I/O subsections. This permits the continual execution of a program without potential interruptions caused by interfacing with the I/O section. The I/O section includes programmable A-to-D and programmable D-to-A converters as well as other circuits for other modes of operation.

d 1 cit ab

1. 5,659,797, Aug. 19, 1997, Sparc RISC based computer system including a single chip processor with memory management and DMA units coupled to a DRAM interface; Frederik Zandveld, et al., 710/22, 26, 105; 711/105 [IMAGE AVAILABLE]

US PAT NO: 5,659,797 [IMAGE AVAILABLE]

L10: 1 of 2

ABSTRACT:

A computer system includes a single-chip central **processor** (20) with handshaking and direct memory access (DMA) controllers for accommodating first and second types of DMA to a dynamic random access memory (DRAM) (34). The single-chip central **processor** (20) has a kernel **processor** (22) having cache, a memory management and control unit (26), and a coprocessor (24). The computer system further includes a **bundle of lines** (28), including data lines, address lines and row address strobe (RAS), column address strobe (CAS), output enable (OE), and write enable (WE) lines for coupling the memory management and control unit (26) to the DRAM (34), and a plurality of data exchanges (33, 37) coupled to a plurality of first and second attach controllers (32, 36). The coprocessor includes a plurality of DMA controllers (240-246) for storing addresses and for storing a length representing a number of data items to be transferred. Additionally, each DMA controller is coupled by a separate line (303) to a respective first attach controller for accommodating a first type of DMA, between the memory and the plurality of data exchanges, which generates addresses of contiguous memory. The plurality of second attach controllers accommodates a second type of DMA between the memory and the plurality of data exchanges. The coprocessor further includes a plurality of handshake controllers (250-256), each for executing handshaking with a respective second attach controller, not under control of the kernel **processor**.